Ruslana Fogler

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EDUCATION

Carnegie Mellon University | GPA 3.82 2021 – 2026
Electrical and Computer Engineering .

Pursuing master's degree until May 2026 | Graduated bachelor's in May 2025.
MS degree funded by Apple New Silicon Initiative Scholarship.

SKILLS

C++/C, Cuda, Python, SystemVerilog, UVM, MATLAB, Java

EXPERIENCE

GPU Shader Core Design Verification Intern May 2025 – Aug 2025
Apple *Austin, TX*

FPGA Platform Engineering Intern May 2024 – Aug 2024
Apple *Cupertino, CA*

PROJECTS

CMU Imaging & Rendering Research *Cuda, C++, Python* October 2024 - December 2025

- Advised by Ioannis Gkioulekas, currenty working on new 3D **neural implicit representation** that enforces **harmonicity** while training . Hoping for submission to SIGGRAPH Asia 2026.
- Wrote **Cuda** algorithms in support of Stochastic Geometry research project

CPU-based Monte Carlo Path Tracer in C++ *C++* Jan 2025 – May 2025

- Coded a path tracer with **next-event estimation**, **multiple important sampling**, various **microfacet BRDFs**, **environment maps**, **volume rendering**, **photon mapping**

3D Structured Light Project *Python* January 2025 - May 2025

- Set up testing scenes and captured data for computational photography (15463) course final project
- Created custom **end-to-end pipeline** of capturing objects under **binary/gray/XOR codes**. Wrote **stereo/projector calibration** code and **post-processing stereo triangulation** from scratch.

GPU Partitioned Audio Convolution for Real Time Applications *Cuda, C++* Jan 2024 – Feb 2024

- Used **Cuda and C++**, wrote uniform partitioned Overlap-Add algorithm with **CuFFT** to convolve massive audio sequences against an impulse reverb in a 2-person team.
- Optimized memory bottleneck with **Cuda Streaming**, achieved over **8x** speedup against sequential methods

RISC-V Processor Core with Cache *SystemVerilog* Jan 2024 - May 2024

- Designed and verified a 5 stage **pipelined RISC-V** with intra/interstage **forwarding and stall**, **hysteresis branch prediction**, and **data cache** in a 3-person team.
- Supports 32 bit-integer RISC-V instruction including all arithmetic, control flow, load/store in immmediate/register formats. Tested with gcc-generated code.

FPGA Gameboy Emulator *SystemVerilog, Altera FPGA* January 2025 - May 2025

- Collaborated on the design, implementation, integration, and validation of a **Gameboy emulator on FPGA** from scratch in a 3-person team. **Won 1st place capstone and David Tuma Best Undergrad Project award**.
- Developed the **MMU**, **APU (Audio Processing Unit)**, and **VGA peripheral RTL modules** to support our custom-built CPU/PPU (Pixel Processing Unit) requests and output display.